

Notice of References Cited	Application/Control No. 10/730,896		Applicant(s)/Patent Under Reexamination PAWLOWSKI, J. THOMAS	
	Examiner Paul R. Myers		Art Unit 2112	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2002/0156953	10-2002	Beiley et al.	710/105
*	B	US-2003/0041223	02-2003	Yeh et al.	711/167
*	C	US-2003/0158981	08-2003	LaBerge, Paul A.	710/100
*	D	US-6,584,526	06-2003	Bogin et al.	710/124
*	E	US-5,630,106	05-1997	Ishibashi, Shohzoh	345/533
*	F	US-6,584,572	06-2003	Choi, Jung-hwan	713/320
*	G	US-6,671,212	12-2003	Macri et al.	365/189.07
*	H	US-2004/0068594	04-2004	Asaro et al.	710/104
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	A 500-MHz 4-Mb CMOS Pipeline-Burst Cache SRAM with Point-to-Point Noise Reduction Coding I/O
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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